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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,779	03/18/2004	Hirofumi Harada	S004-5242	8062

7590 11/15/2005

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/803,779	HARADA, HIROFUMI	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 and 6 is/are rejected.

7)☒ Claim(s) 2-5 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 18 March 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 2 should be designated by a legend such as --**Prior Art**-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawing is objected to because the reference numbers "6" and "9" disclosed in Fig. 12 have been incorrectly labeled the elements. Therefore, in Fig. 12, the reference number "6" should be changed to "9" which refers to an intermediate insulating film, and the reference number "9" should be changed to "6" which refers to polycrystalline silicon gate electrode.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Kocon et al. (U.S. Pat. 6,351,009).

Regarding claim 1, APA (Fig. 2) discloses a vertical MOS transistor comprising: a semiconductor substrate 1 of a first conductivity type (see Specification, page 1, lines 10-11); an epitaxial growth layer 2 of the first conductivity type which is formed on the semiconductor substrate 1 (see Specification, page 1, lines 8-11); a body region 3 of a second conductivity type which is formed on the epitaxial growth layer 2 (see

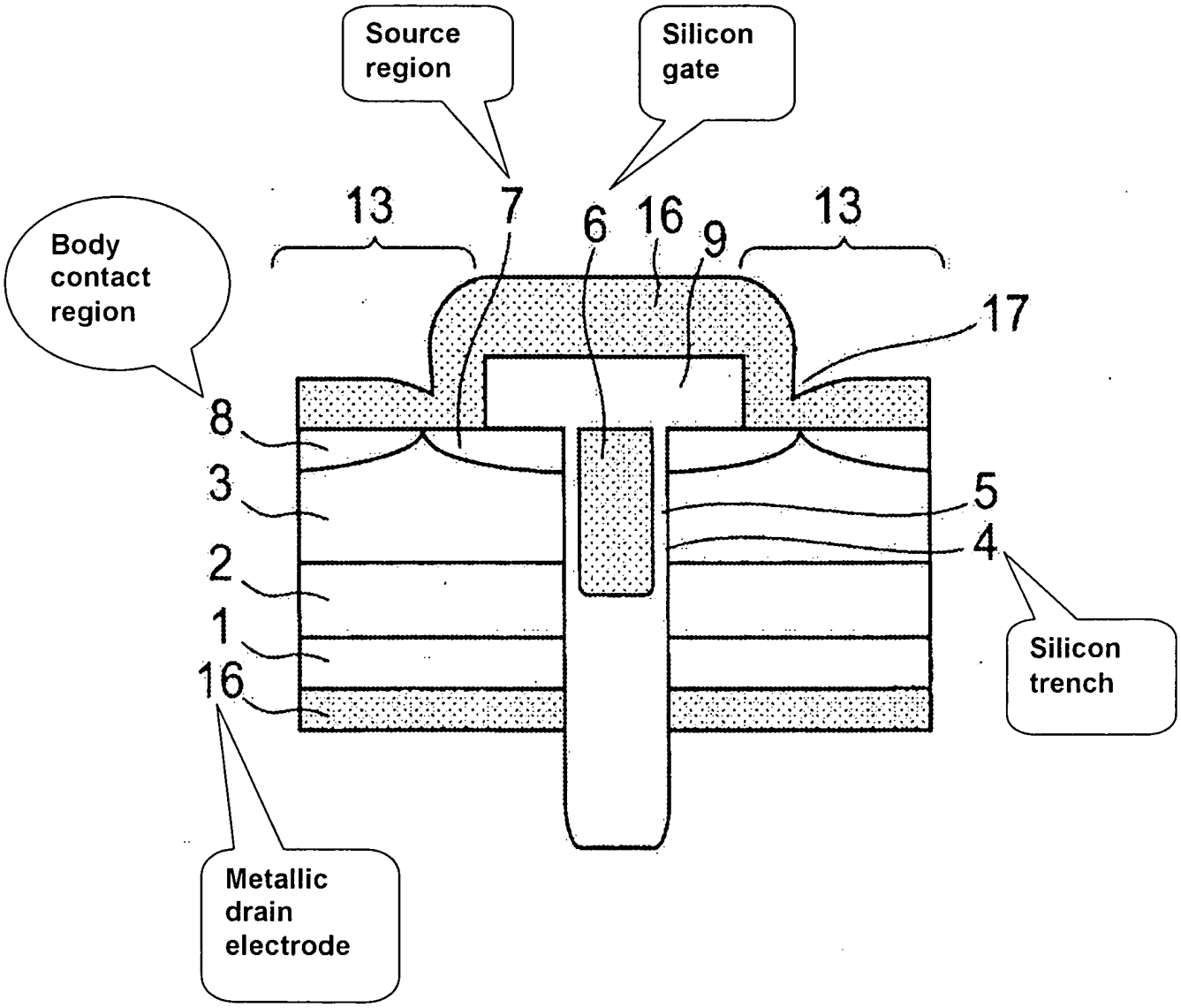
Specification, page 1, lines 14-17); a heavily doped body contact region 8 of the second conductivity type which is formed on a part of a surface of the second conductivity type body region 3 (see Specification, page 1, lines 18-21); a heavily doped source region 7 of the first conductivity type (see Specification, page 1, lines 18-20), which is formed on a part of the surface of the second conductivity type body region that is covered with the heavily doped body contact region 8 (see Fig. 2 labeled by the examiner below); a silicon trench 4 piercing the second conductivity type body region 3 and the first conductivity type source region 7 to reach an inner part of the first conductivity type epitaxial growth layer 2 (Specification, page 2, lines 6-8); a gate insulating film 5 formed along walls and bottom of the silicon trench 4 (Specification, page 2, line 8); a heavily doped polycrystalline silicon gate 6 buried in the silicon trench 4 while surrounded by the gate insulating film 5 (Specification, page 2, lines 8-10); an intermediate insulating film 9 formed on the polycrystalline silicon gate 6 in the silicon trench 4 to reach a surface the semiconductor substrate 1; a metallic source electrode 16 being in contact with the intermediate insulating film 9, the heavily doped source region 7, and the heavily doped body contact region 8; and a metallic drain electrode 16 connected to a rear surface of the semiconductor substrate 1 (see Fig. 2 labeled by the examiner below).

APA does not disclose a heavily doped polycrystalline silicon gate 6 buried in the silicon trench 4 to a level of the first conductivity type source region 7.

However, Kocon (Fig. 2) teaches a MOS- gated device 200 having a gate material 210, which is recessed within the trench 207 to a level of the first conductivity

type source region 206 to permit the inclusion of an intermediate insulating film 212 of sufficient thickness to provide gate isolation (column 3, lines 36-38). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device structure of APA by forming the silicon gate buried in the silicon trench to a level of the source region because such a forming the silicon gate buried in the silicon trench to a level of the source region would eliminate the surface area required for gate-source dielectric isolation and reduce the device size, as taught by Kocon (column 3, lines 10-13).

FIG. 2 (PRIOR ART)



Regarding claim 6, APA does not disclose that the heavily doped polycrystalline silicon gate buried in the silicon trench is 0.5 μm to 1.0 μm down from the top of the trench.

However, Kocon (Fig. 2) teaches a MOS- gated device 200 having a gate material 210, which is recessed within the trench 207 to permit the inclusion of an intermediate insulating film 212 of sufficient thickness to provide gate isolation (column 3, lines 36-38). In additional, Kocon teaches a typical minimum thickness of about 0.5 μm to 0.8 μm for dielectric layer 111 that imposes limitations on the minimum size of device 100 (see Fig. 1). It would be desirable to be able to reduce the size and improve the efficiency of semiconductor devices (column 2, lines 1-9). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the device structure of APA by forming the heavily doped polycrystalline silicon gate buried in the silicon trench is 0.5 μm to 1.0 μm down from the top of the trench would be able to reduce the size and improve the efficiency of semiconductor devices, as taught by Kocon (column 2, lines 1-9). Furthermore, it has been held that when the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Allowable Subject Matter

5. Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose all the limitations recited in the above claims. Specifically, the prior art of record fails to disclose an insulator, which is provided on the sidewalls of the silicon trench above the heavily doped polycrystalline silicon gate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
November 9, 2005.

PHAT X. CAO
PRIMARY EXAMINER